PLL Clock Multiplier

Features

- Low cost frequency multiplier
- Zero ppm multiplication error
- Input crystal frequency of 5 - 30 MHz
- Input clock frequency of 4 - 50 MHz
- Output clock frequencies up to 180 MHz
- Period jitter 50ps (100~180MHz)
- Duty cycle of 45/55% up to 160MHz
- Operating voltages of 3.0 to 5.5V
- Tri-state output for board level testing
- Die form, Wafer form

Applications

- Used for crystal oscillator

Description

The PT7C4502 is a high performance frequency multiplier, which integrates Analog Phase Lock Loop techniques.

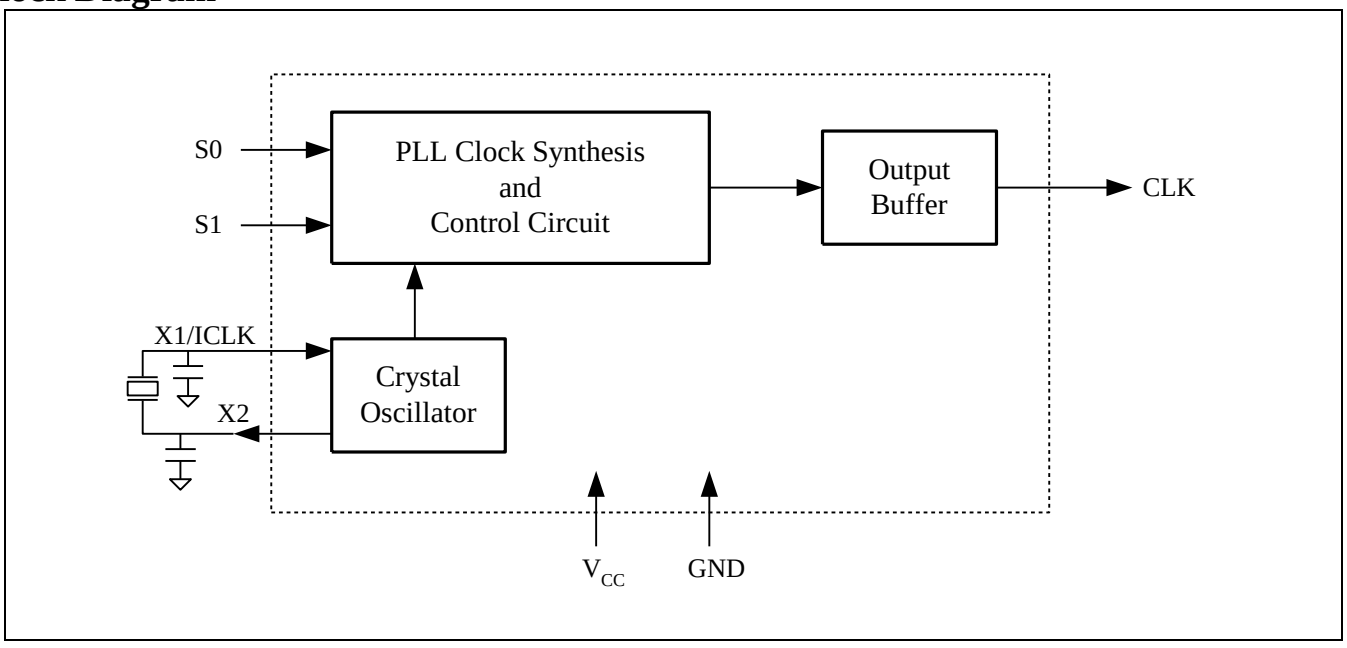
The PT7C4502 is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. It is designed to replace crystal oscillators in most electronic systems, clock multiplier and frequency translation.

Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 180 MHz.

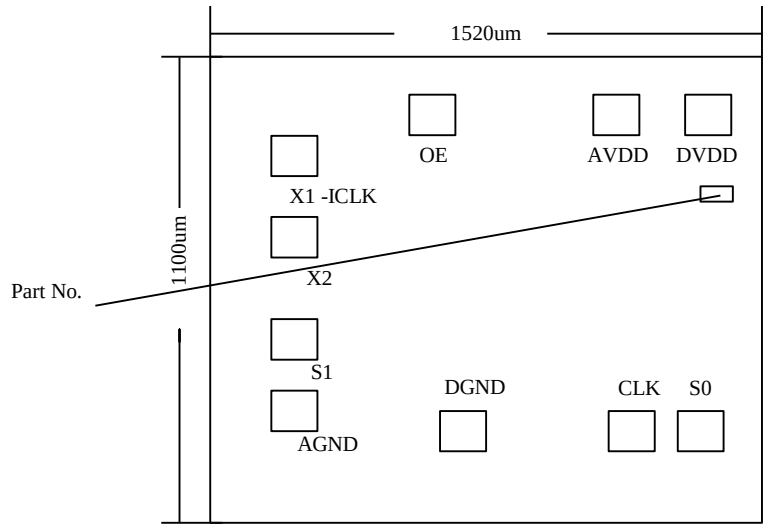
The complex Logic divider is the ability to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

The device also has an Output Enable pin that tri-states the clock output when the OE pin is taken low. This product is intended for clock generation and frequency translation with low output jitter (variation in the output period)

Block Diagram



Pin/Pad Configuration



Pin/Pad Description

Pin Name	Pad Name	Type	Description
X1/ICLK	X1-ICLK	I	Crystal connection or clock input.
X2		O	Crystal connection. Leave unconnected for clock input.
S0		I	Multiplier select pin 0. Connect to Vcc or float.
S1		I	Multiplier select pin 1. Connect to GND or float. Internal pull-up.
OE		I	Output Enable. Tri-states CLK output when low.
CLK		O	Clock output.
VCC	AVDD	P	Analog Power.
	DVDD	P	Digital power.
GND	AGND	P	Analog Ground
	DGND	P	Digital ground.

Pad Coordinate File					
Pad Name	X Coordinate	Y Coordinate	Pad Name	X Coordinate	Y Coordinate
X1-ICLK	120.90	892.90	CLK	1098.90	118.60
X2	120.90	641.50	S0	1322.10	118.60
S1	117.70	401.10	DVDD	1303.50	973.30
AGND	111.50	225.80	AVDD	1063.10	973.30
DGND	698.40	118.60	OE	470.70	981.70
Note: Substrate is connected to GND.					
Die Size: 1670μm*1180μm (Including scribe line size 150μm*80μm.) **Die Thickness:** PT7C4502DE: 350±25μm without coating; PT7C4502-2WF: 220±20μm with coating **Pad Size:** 75μm*75μm					

S1	S0	CLK
0	M [Note 2]	×2 [Note 1]
0	1	×3
1 [Note 3]	M [Note 2]	×4 (default)
1 [Note 3]	1	×5

Note 1: CLK output frequency=ICLK×2;
2. M=Leave unconnected (self-biases to Vcc/2);
3. Internal pull-up on S1, unconnected = 1

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the PT7C4502 must be isolated from system power supply noise to perform optimally. A decoupling capacitor of 0.01μF or 0.1uF must be connected between VCC and the GND. It must be connected close to the PT7C4502 to minimize lead inductance. No external power supply filtering is required for the PT7C4502.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Load Capacitors

There is no on-chip capacitance build-in chip. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal C_L*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 15 pF load capacitance, each crystal capacitor would be 30pF.

Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Supply Voltage to Ground Potential (V_{CC}) ..... -0.3V to + 7.0V
Inputs(Reference to GND) ..... -0.5V to Vcc + 0.5V
Clock Output (Reference to GND) ..... -0.5V to Vcc + 0.5V
Soldering Temperature (Max of 10 seconds) ..... 260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Description	Min	Type	Max	Unit
T_A	Operation Temperature	-40	-	+85	°C
V_{DD}	Supply voltage	3.0	-	5.5	V

DC Electrical Characteristics

(V_{CC} = 3.3V ± 0.3V, T_A = -40 ~ 85℃, unless otherwise noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	-	Vcc	3	3.3	3.6	V
Icc	Supply Current	no load, 20MHz crystal, OE = Vcc	Vcc	-	12	20	mA
V_{IH}	Input Logic High	-	ICLK, OE	2	-	-	V
V_{IL}	Input Logic Low	-	ICLK, OE	-	-	0.8	V
V_{IH}	Input Logic High	-	S0, S1	Vcc-0.5	-	-	V
V_{IM}	Input mid-level	-	S0, S1	-	Vcc/2	-	V
V_{IL}	Input Logic Low	-	S0, S1	-	-	0.5	V
V_{OH}	High-level output voltage	I_{OH} = -12mA	CLK	2.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = 12mA	CLK	-	-	0.4	V
I_S	Short Circuit Current	-	CLK	-	±30	-	mA
I_I	Input Leakage Current	-	OE	-	–	1	µA
		-	S1	-	-7.5	-20	µA

(V_{CC} = 5.0V ± 0.5V, T_A = -40 ~ 85℃, unless otherwise noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	-	Vcc	4.5	5.0	5.5	V
Icc	Supply Current	no load, 20MHz crystal, OE = Vcc	Vcc	-	20	30	mA
V_{IH}	Input Logic High	-	ICLK, OE	0.65Vcc	-	-	V
V_{IL}	Input Logic Low	-	ICLK, OE	-	-	0.8	V
V_{IH}	Input Logic High	-	S0, S1	Vcc-0.4	-	-	V
V_{IM}	Input mid-level	-	S0, S1	-	Vcc/2	-	V
V_{IL}	Input Logic Low	-	S0, S1	-	-	0.4	V
V_{OH}	High-level output voltage	I_{OH} = -12mA	CLK	Vcc-0.5	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = 12mA	CLK	-	-	0.4	V
I_S	Short Circuit Current	-	CLK	-	±70	-	mA
I_I	Input Leakage Current	-	OE	-	–	1	µA
		-	S1	-	-7.5	-20	µA

AC Electrical Characteristics

(V_{CC} = 3.3V ± 0.3V, T_A = -40 ~ 85℃, unless otherwise noted)

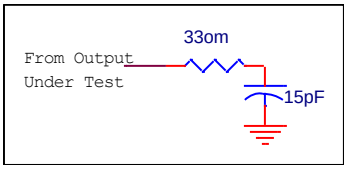
Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	Crystal	ICLK	5	-	30	MHz
f_{OUT}	Output frequency	Vcc: 3.0 to 3.6V	CLK	20	-	180	MHz
t_r	Output clock rise time	0.8 to 2.0V, 15pF load	CLK	-	1	-	ns
t_f	Output clock fall time	2.0 to 0.8V, 15pF load	CLK	-	1	-	ns
Duty	Output clock duty cycle	At Vcc/2, below 160MHz	CLK	45	50	55	%
		At Vcc/2, 160MHz to 180MHz	CLK	40		60	%
	PLL bandwidth	-	-	10	-	-	kHz
	Output enable time	OE high to output on	-	-	-	50	ns
	Output disable time	OE low to tri-state	-	-	-	50	ns
	Period Jitter	100MHz~180MHz	CLK	-	50	100	ps

(V_{CC} = 5.0V ± 0.5V, T_A = -40 ~ 85℃, unless otherwise noted)

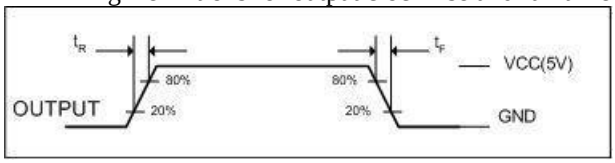
Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	Crystal	ICLK	5	-	30	MHz
f_{OUT}	Output frequency	Vcc: 4.5 to 5.5V	CLK	20	-	180	MHz
t_r	Output clock rise time	20%Vcc to 80%Vcc, 15pF load	CLK	-	1.2	-	ns
t_f	Output clock fall time	20%Vcc to 80%Vcc, 15pF load	CLK	-	1.2	-	ns
Duty	Output clock duty cycle	At Vcc/2, below 160MHz	CLK	45	50	55	%
		At Vcc/2, 160MHz to 180MHz	CLK	40		60	%
	PLL bandwidth	-	-	10	-	-	kHz
	Output enable time	OE high to output on	-	-	-	50	ns
	Output disable time	OE low to tri-state	-	-	-	50	ns
	Period Jitter	100MHz~180MHz	CLK	-	50	100	ps

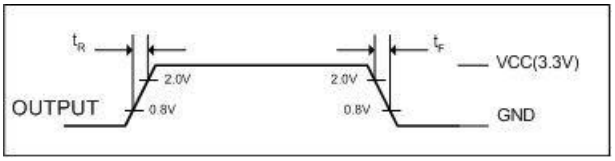
Test circuits

1>Load circuit for output clock duty cycle, rise and fall time Measurement



2>Timing Definitions for output clock rise and fall time Measurement





Ordering Information

Part Number	Package Code	Package
PT7C4502DE	DE	350±25μm without coating Die form
PT7C4502-2WF	WF	220±20μm with coating Wafer form

Note:

- E = Pb-free and Green
- "-2" shows die thickness is 220±20μm with coating; PT7C4502DE die thickness is 350±25μm with coating.
- Adding X Suffix= Tape/Reel